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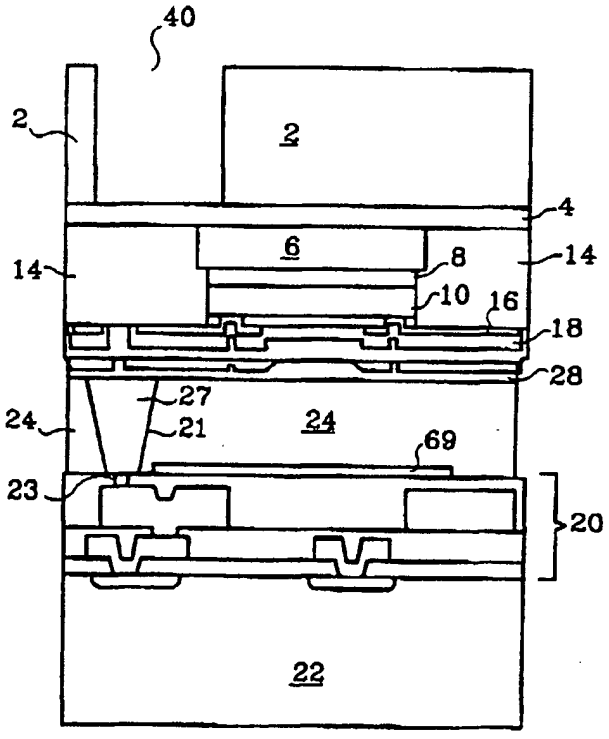
(54) Title: DUAL WAFER ATTACHMENT PROCESS



(57) Abstract: Producing the microstructures on separate substrates, which are bonded. One of these structures may be temperature sensitive CMOS electronics. There may be a high-temperature thermal sensor on one wafer and low-temperature CMOS electronics. In the case where the bonding material is polyimide, the polyimide on both surfaces to be bonded is soft baked. The wafers are placed in a wafer bonder and, using precision alignment, brought into contact. The application of pressure and heat forms a bond between the two coatings of polyimide. A wafer may need to be removed from a combined structure. One of the bonded structures may be placed on a sacrificial layer that can be etched away to facilitate removal of a wafer without grinding. After wafer removal, a contact from the backside of one of the structures now on polyimide to the other on the wafer may be made. Sacrificial material, for example, polyimide, may be removed from between the structures that are connected via a contact. A microstructure may be bonded with something that is not a microstructure, such as single-or multi-layer material, crystalline or amorphous.

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DUAL WAFER ATTACHMENT PROCESS

BACKGROUND

The Government may have rights in this invention pursuant to Contract No. N00014-96-C-2906, awarded by the Department of the Navy.

The invention pertains to microstructure wafers. Particularly, it pertains to attachment of wafers, and more particularly to temperature sensitive wafers.

The invention involves the bonding of devices or materials fabricated on separate wafers. A microstructure's front surface may be bonded to another microstructure; however, a microstructure on one substrate may be incompatible with the process used to produce the other microstructure. The invention is designed to avoid problems caused by such incompatibility.

The need for such a process is driven by the performance needs in several areas of military and industrial applications, including thermal and mechanical sensors, magnetoresistive memory arrays, and superconducting channels.

Wafer bonding technology has existed for some time. Therefore, other patented processes exist producing more and less similar structures. The idea of bonding wafers

processed with incompatible processes has been tried. Existing bolometer technology requires that the readout electronics, CMOS and metalizations survive the processing conditions used for the detector materials. The development of high temperature coefficient of resistance (TCR) materials, which require very high processing temperature, provided an incentive to develop a technique for coupling these materials into bolometer technology. The present technique is superior to related art single-wafer technology because the detector film is processed at temperatures much higher than 450 degrees Celsius (C), which is the practical limit of CMOS devices.

SUMMARY OF THE INVENTION

The present invention consists of producing the desired microstructures on separate substrates and coating them with a suitable bonding material. These structures may be CMOS electronics or a pure microstructure. One embodiment includes a high-temperature thermal sensor on one wafer and low-temperature CMOS electronics with some electrical and thermal features on another wafer. In the case where the bonding material is polyimide, the polyimide on both surfaces to be bonded are soft baked. The wafers are placed in a wafer bonder and, using precision alignment, brought

into contact. The application of pressure and heat forms a bond between the two coatings of polyimide.

A wafer may need to be removed from a combined structure. A particularly advantageous technique is to build one of the bonded structures on a sacrificial layer that can be etched away to facilitate removal of a wafer without grinding. Further processing can be done on either or both structures.

After wafer removal, a contact from the backside of one of the structures now on polyimide to the other on the wafer has been demonstrated. This contact, electrical or physical, is one of many kinds, which could be made. Sacrificial material, for example, polyimide, may be removed from between the structures that are bonded via a contact. It may also be desirable to bond a microstructure with something that is not a microstructure, such as single- or multi-layer material, crystalline or amorphous. The present process provides a good method of bonding of these items, while incorporating the materials having a temperature coefficient of resistance that range from a typical value of 2 %/C to a high value of 3.5 %/C on the present wafers. The TCR may be measured at a value of 12 %/C on bulk substrates with much lower 1/f ($k=10^{-14}$) noise than VO_x (vanadium oxide) ($k=10^{-13}$) films. The material may be thinned after wafer removal to improve performance with lower mass.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-6 are cross-sectional views of a high-temperature thermal sensor being formed on a silicon wafer.

Figures 7-10 are cross-sectional views of an adaptive structure being formed over CMOS electronics on a silicon wafer.

Figure 11 shows the sensor and electronics after having been bonded together.

Figures 12-13 demonstrate a certain method of removing a silicon wafer, using a sacrificial layer, after the structures have been bonded.

Figure 14 demonstrates further processing on the structure formed on the removed wafer.

Figure 15 shows the removal of part of the original bonding mediums.

Figure 16 shows the removal of dielectric material in a region into which a contact is to be deposited.

Figure 17 shows the deposition of a structural and electrical contact on the final bonding medium.

Figure 18 shows the removal of other sacrificial material.

Figure 19 shows the deposition of a reflector and a polyimide sacrificial layer on the wafer.

Figure 20 shows an attachment of two wafers via their polyimide layers.

Figure 21 shows the etch of an access hole through a silicon wafer to an etch stopping layer.

Figure 22 shows the removal of the silicon wafer with the removal of the etch stopping layer of Figure 21.

Figure 23 reveals a YSZ crystal orientation layer and the polyimide layer thinned by milling.

Figure 24 shows the removal of the polyimide layer and a punch-through of another polyimide layer to contacts or reflectors of electronic devices.

Figure 25 reveals a self-aligned cut of dielectric layers.

Figure 26 shows a structural and electrical contact between a reflector or contact of the electronic devices and the leg metal.

Figure 27 reveals the removal of the sacrificial polyimide resulting in a thermal isolation between the leg metal and the device electronics.

Figure 28 is a planar view of a pixel use in the resultant device of the dual wafer attachment process.

DESCRIPTION OF THE EMBODIMENTS

The dual wafer microstructure attachment process (DWaMA Process) is described in the context of fabricating a

bolometer. The process, in this context and in general, is partitioned into three phases of fabrication.

The first phase is to create a microstructure for thermal sensing. A high temperature coefficient of resistance (TCR) film is necessary for high performance microstructures, requiring high temperature processing. The microstructure will be formed on a first, temporary wafer on which a release layer will first be deposited. These steps are illustrated in Figures 1-6 for one device of many on a given wafer.

In Figure 1, a silicon wafer 2 of a suitable quality is obtained and prepared to be used as a substrate for a thermal sensing microstructure. A layer 4 of hastalloy is first deposited across the surface of wafer 2. This material is compatible with the processes required to form the sensor, though it is not part of it, and can be etched by a method with good selectivity properties against the materials to be in contact with it, excluding the wafer. It also provides a suitable surface on which to form the sensor. Any material used for this sacrificial layer should have these three properties. A yttria stabilized zirconia (YSZ) crystal orientation film 6, appropriate for the application, is then deposited across the surface of hastalloy layer 4 and patterned, leaving a mesa 6, per this particular sensor's design. Since this wafer's front

surface will be bonded with another's front surface, the sensor is actually being constructed from the top down. This property of the proposed method can be considered when designing according to this methodology. Present wafer 2 is designed according to the mirroring effect, which takes place when bonding wafers face-to-face.

A layer 8 of Bi_xTiO_y is deposited on the exposed areas of hastalloy layer 4 as well as on the surfaces of the YSZ mesa 6, using a solgel process, as shown in Figure 2. On Bi_xTiO_y layer 8, a CMR (colossal magneto-resistance) film 10 is deposited on all surfaces with a solgel process and the best thermal processing available. A Si_3N_4 layer 12 is deposited on CMR film 10, thereby passivating the film.

A photoresist is applied to the surface of Si_3N_4 layer 12, and patterned to form a mesa of layers Bi_xTiO_y 8, CMR 10, and Si_3N_4 12 on YSZ 6 mesa. A subsequent etch of these three layers on the YSZ and hastalloy layers 6 and 4. Polyimide 14 is deposited to a depth greater than the height of the entire mesa and is planarized to the level of the mesa, with the resulting structure in Figure 3.

Si_3N_4 layer 12 is patterned in the same way, using a mask defining contacts to CMR film 10, as shown in Figure 4. Metal 16 is deposited and patterned such that polyimide layer 14 is exposed in region 15 in the areas where layers 6, 8, 10, and 12 were previously removed. The width of the

CMOS devices 20 are formed on a first silicon wafer 22, being depicted in Figure 7. A reflector 69 is deposited and patterned on top of the CMOS devices 20 to define the optical cavity between the reflector and the microstructure above it. A thick layer of polyimide 24 is deposited and patterned, producing a basket 21 above a CMOS lead 23 for the purpose of providing a form for metal to be deposited. Polyimide layer 24 also acts as a sacrificial layer, occupying a space between electronics 20 and the microstructure.

Aluminum 26 is deposited across the entire surface of polyimide layer 24, as seen in Figure 8, making electrical contact with lead 23 at the bottom of basket 21, and thus to electronics 20, and filling basket 21 to a level above the level of polyimide layer 24.

Aluminum post 27 is planarized in Figure 9 by means of a chemical mechanical polish (CMP). This CMP is of a duration so as to re-expose polyimide 24 but not thin it a significant amount.

A polyimide layer 28 is deposited across the surfaces of planarized polyimide 24 and aluminum post 27, as shown in Figure 10. This polyimide layer 28 is partially cured by baking at 100° C for two minutes. The thickness of this layer is nominally about 1000 angstroms, but may need to be

thicker in the presence of a non-planar surface. This temporarily completes processing on wafer 22.

The first half of the third and final phase is to attach the high temperature microstructure film to the CMOS devices by bonding polyimide layers 19 and 28, respectively, which are the top layers on each wafer. This is shown in Figure 10. Next, wafer 2 is removed to allow exposure of the sensor.

Being coated with soft-baked polyimide, the wafers are aligned to within one micron of their front surfaces opposite each other in a wafer-to-wafer bonding apparatus while being held a few microns (e.g., < 100 microns) apart. They are fused together with the application of pressure and heat. Here is the essence of the present invention. This process discloses a simple method to bond these two structures. Also, it is a wafer level process that enables a quarter of a million devices to be fabricated in parallel. Pressures can range from 20 to 100 psi, 60 psi being nominal. Temperatures don't exceed 400 degrees C. Temperatures should not exceed 450 degrees C when microelectronics are involved. The bonding process is done either in a vacuum or in the presence of non-oxidizing or inert gases. The resulting cross section is seen in Figure 11.

Access holes 40 are cut into temporary second wafer 2 from the back side using a deep RIE (reactive ion etch) silicon etch, stopping on hastalloy release layer 4, as seen in Figure 12. These holes provide local exposure to hastalloy layer 4, thereby allowing the hastalloy to be etched in a shorter period of time. The release layer is chemically etched to allow the removal of temporary wafer 2 from the bonded assembly, being shown in Figure 13.

YSZ crystal orientation layer 6 and surrounding polyimide layer 14 are thinned by a means of blanket milling to a thickness as desired for the sensor. Figure 14 illustrates this.

The second half of the third and final phase is to open a region between the microstructure and post 27 created on the readout wafer, make an electrical and physical connection, and remove sacrificial polyimide layers 19, 24 and 28, so as to provide thermal isolation between the microstructure and the readout substrate.

Figure 15 displays the bonded assembly after some of the polyimide 14, 19, 24 has been removed. The anisotropic etch removes a portion of polyimide 14 layer at the surface of the structure and is allowed to continue through space 15 in metal 16. The etchant stops at aluminum post 27 while removing portions of polyimide layers 19 and 28 that had

been at the surface of the wafers at the time of bonding and below space 15.

A cut, self-aligned to YSZ film 6 and leg metal 16, is made of dielectric layer 18 in region 42, as demonstrated in Figure 16.

The second-to-last stage of processing involves depositing and patterning an electrical and structural contact 44 in the discussed region 42, affixed to post 27 and leg metal 16. Figure 17 shows the contact.

Finally, Figure 18 shows the final product after a dry etch has removed the remaining parts of polyimide layers 24, 28, 19, creating the final desired thermal isolation.

The above procedure can be modified to eliminate the use of post 27. The following illustrates that modification. In Figure 19, as in Figure 1, reflector 69 is deposited and patterned on top of CMOS electronics 20 and their interconnect metals 50 to form the optically resonant cavity between the reflector deposited and patterned on top of wafer 22 and the microstructure of wafer 2. A layer of polyimide 51 is deposited on top of the resulting structure, but here it is not patterned or etched.

As before, wafers 2, 22 of Figures 19 and 20, respectively, are bonded. Holes 52 are etched to hastalloy layer 53 through wafer 2, as shown in Figure 21. Wafer 2 is removed with an etch of hastalloy layer 53 in Figure 22.

YSZ crystal orientation layer 56 is thinned by blanket milling along with polyimide layer 54 in Figure 23.

In Figure 24, as in Figure 15, polyimide layer 54 and portions of layers 51 and 60 are etched, exposing leg metal 58 and punching through to CMOS lead 50, which is electrically connected to CMOS devices 20.

A cut of dielectric layer 62, self-aligned to YSZ film 56 and leg metal features 58, is made and is shown in Figure 25.

Finally, contact 64 is deposited and patterned, making electrical and structural contact between CMOS lead metal 50 and leg metal 58, of Figure 26. Remaining polyimide layers 51 and 60 are etched away, in Figure 27. The resulting assembly uses only one deposited material to make the backside contact from leg metal 58 to CMOS lead metal 50.

The above procedure can be further modified to substitute the use of hastalloy with molybdenum for faster etching. Molybdenum requires less etching time for release but may not promote crystalinity in the YSZ and thereby the CMR films as well as hastalloy.

Figure 28 reveals a plan view of a pixel of the resultant device of the described process. It shows reflector 69, YSZ 6 and CMR resistor 10. Also, contacts 44 and 64, and leg metals 16. This figure shows interconnects

71, which are not shown in the cross-section view of the device, to pads.

This process allows the separation of the non-CMOS-compatible process steps, which in this case is the high temperature processing of the sensor material, from those needed to form CMOS electronics. It also demonstrates the assembly of these structures through thin film contact layers and sacrificial release layers. Although the process has been described using CMOS and non-CMOS processes, a much broader range of applications can be made.

Though the invention has been described with respect to a specific preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore intended that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

THE CLAIMS

1. A process for attaching first and second wafers, at least one wafer having a microstructure, comprising:

making a first wafer having low-temperature microelectronics, having a first set of connections;

making a second wafer at a high temperature having a second set of connections mirrored to match the first set of connections;

applying a polyimide layer on a topside of said first wafer;

applying a polyimide layer on a topside of said second wafer;

soft baking said first and second wafers;

facing the topsides of said first and second wafers with each other;

aligning said first and second wafers to each other;

bonding said first and second wafers together under a pressure at a temperature in a non-oxidizing environment;

etching holes through said polyimide layers down to sets the respective of connections; and

sputtering a conductive material into the holes so as to make contact to the sets of connections.

2. A process for a temperature sensitive wafer with a wafer processed at a high temperature, comprising:

forming a hastalloy layer on a first silicon wafer;

forming a YSZ film layer on the hastalloy layer;

patterning and etching the YSZ layer;

forming a Bi_xTiO_y layer on the YSZ layer;

forming a CMR layer on the Bi_xTiO_y layer;

forming a silicon nitride layer on the CMR layer;

patterning and etching the silicon nitrate, CMR and Bi_xTiO_y layers into a resister pattern;

forming a first polyimide layer on the silicon nitride layer and a portion of the hastalloy layer;

planarizing the first polyimide layer to the silicon nitride layer;

cutting a first via through the silicon nitride layer to the CMR layer;

forming a metal layer that fills the first via to contact the CMR layer;

patterning and etching the metal layer;

forming a dielectric layer on the metal layer;

etching a second via through the dielectric and metal layers to the first polyimide layer;

forming a second polyimide layer on the dielectric layer;

forming CMOS electronics on a second silicon wafer;

forming a third polyimide layer on the CMOS electronics;

patterning and etching a third via through the third polyimide layer to the CMOS electronics;

forming a metal layer that fills the third via to contact the CMOS electronics, on the third polyimide layer;

planarizing the metal layer to the third polyimide layer;

forming a fourth polyimide layer on portions of the third polyimide layer and the metal layer;

aligning first and second wafers, having the second and fourth polyimide layers proximate to each other;

press-bonding the second and fourth polyimide layers to each other;

cutting an access hole through the first silicon wafer to the hastalloy layer;

etching away the hastalloy layer to release the first silicon layer;

milling the first polyimide layer and the YSZ layer to thin the YSZ layer;

removing the first polyimide layer;

removing a portion of the second and fourth polyimide layers to provide a path via the second via to the metal layer situated in the third via;

forming a contact post in the second via to the metal layer situated in the third via; and

remove the second, third and fourth polyimide layers;

wherein the contact post and the metal layer situated in the third via provide structural support and thermal isolation between the YSZ, Bi_xTi0_y, CMR and silicon nitride layers and the CMOS electronics and second silicon wafer.

3. A process for attaching a temperature-sensitive wafer to high temperature wafer, comprising:

forming a hastalloy layer on a first wafer;

forming a YSZ layer on the hastalloy layer;

patterning and etching the YSZ layer;

forming a titanate layer on the YSZ layer;

forming a CMR layer on the Bi_xTi0_y layer;

forming a first dielectric layer on the CMR layer;

patterning and etching the first dielectric, CMR and titanate layers into a resistor pattern;

forming a first polyimide layer on the first dielectric layer and a portion of the hastalloy layer;

planarizing the first polyimide layer to the first dielectric layer;

cutting a first via through the first dielectric layer to the CMR layer;

forming a metal layer that fills the first via to contact the CMR layer;

patterning and etching the metal layer forming a second dielectric layer on the metal layer;

etching a second via through the second dielectric and metal layers to the first polyimide layer;

forming a second polyimide layer on the dielectric layer;

forming CMOS on a second wafer;

forming a third polyimide layer on the CMOS;

aligning the first and second wafers and having the second and third polyimide layers proximate to each other;

press-bonding the second and third polyimide layers to each other;

cutting an access hole through the first wafer;

removing the hastalloy layer via the access hole to release the first wafer;

removing the first polyimide layer;

punching a hole through the second via and second and third polyimide layers to the CMOS;

forming a contact post through the metal layer, dielectric layer, and second and third polyimide layers via the hole; and

removing the second and third polyimide layers to result in thermal isolation between the CMOS and the metal layers.

4. A process for attaching first and second wafers comprising:

forming a first microstructure on the first wafer;

forming a second microstructure on the second wafer;

coating the first microstructure with a first bonding material having a first thickness;

coating the second microstructure with a second bonding material having a second thickness;

aligning the first and second wafers;

bringing the first and second bonding materials into contact;

and fusing the coatings and forming a bond between the first and second bonding materials and between the first and second microstructures such that the first and second thicknesses of the first and second bonding materials, respectively, determine a separation between the first and second microstructures.

5. The process of claim 4, wherein the first wafer is silicon.

6. The process of claim 5, wherein the second wafer is made of silicon.

7. The process of claim 6, wherein the first microstructure formed on the first wafer is microelectronics.

8. The process of claim 7, wherein the first and second bonding materials are polyimide.

9. The process of claim 8, wherein the first and second thicknesses of the first and second bonding materials, respectively, are approximately equal.

10. The process of claim 9, wherein the fusing the coatings is followed by removing the bonding materials.

11. The process of claim 1, wherein the fusing the coatings is followed by removing the second wafer.

12. The process of claim 11, wherein the removing the second wafer comprises removing a sacrificial layer to separate the second wafer from the second microstructure.

13. The process of claim 12, wherein the removing a sacrificial layer is preceded by a forming of an access to the sacrificial layer.

14. The process of claim 13 further comprising forming a contact from the first microstructure to the second microstructure.

15. The process of claim 14, wherein the contact is formed from a backside of one of the first or second microstructures.

16. The process of claim 15, further comprising fusing additional wafers, having microstructures and coated with bonding material, to the existing bonded microstructures.

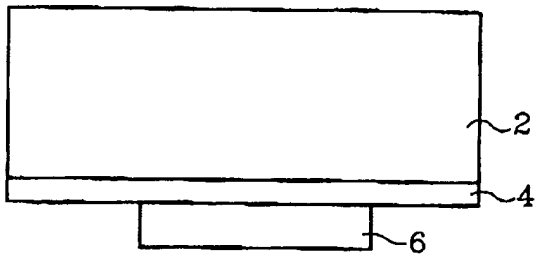

Fig.1

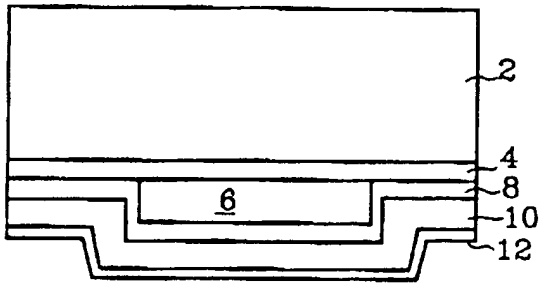

Fig.2

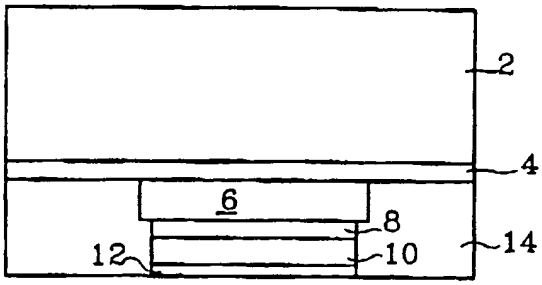

Fig.3

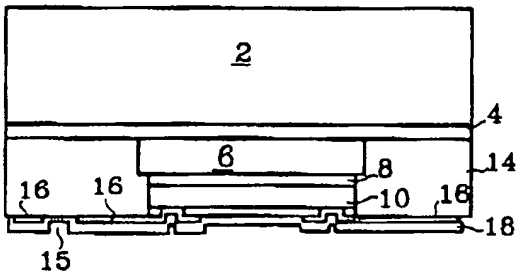

Fig.4

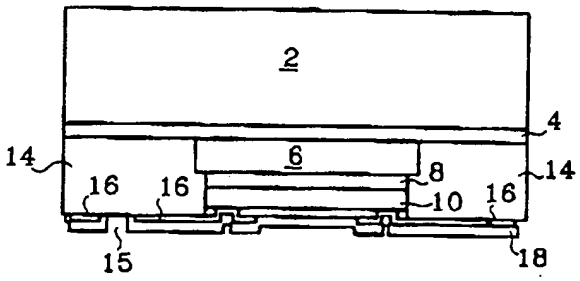

Fig.5

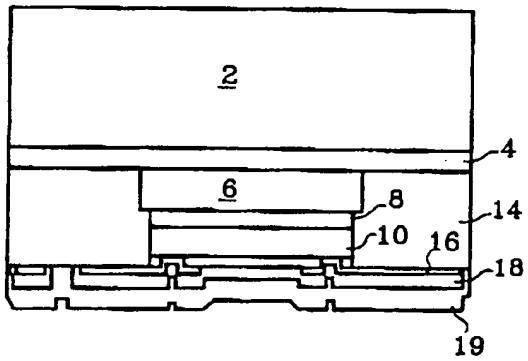

Fig.6

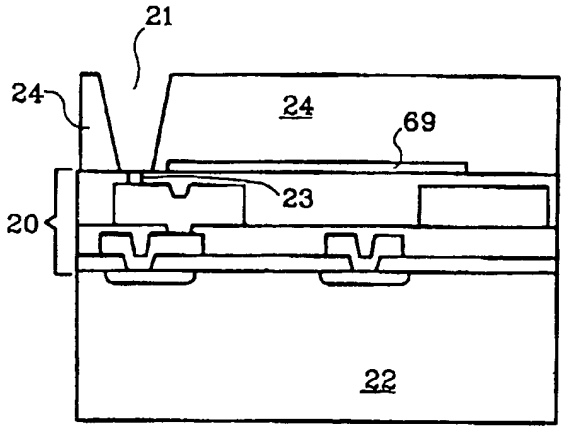

Fig. 7

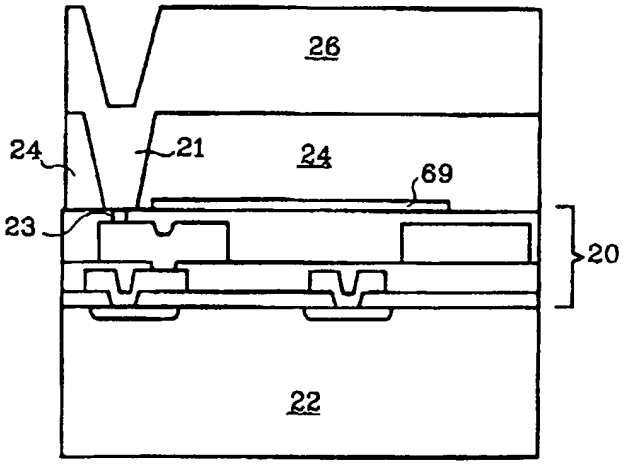

Fig. 8

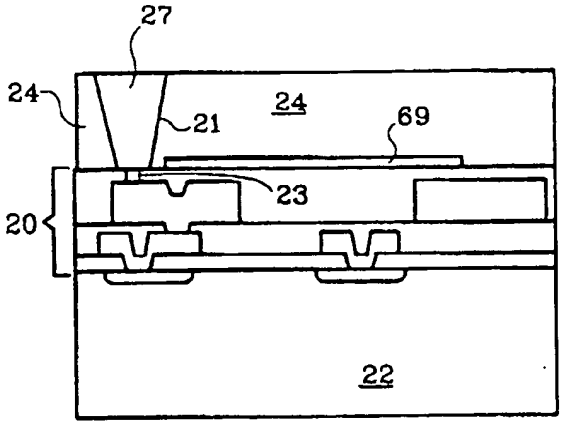

Fig.9

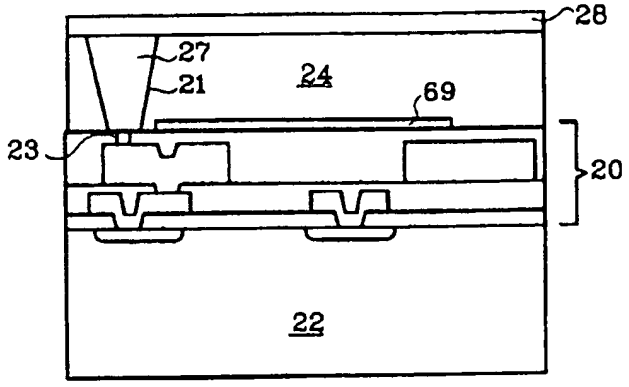

Fig.10

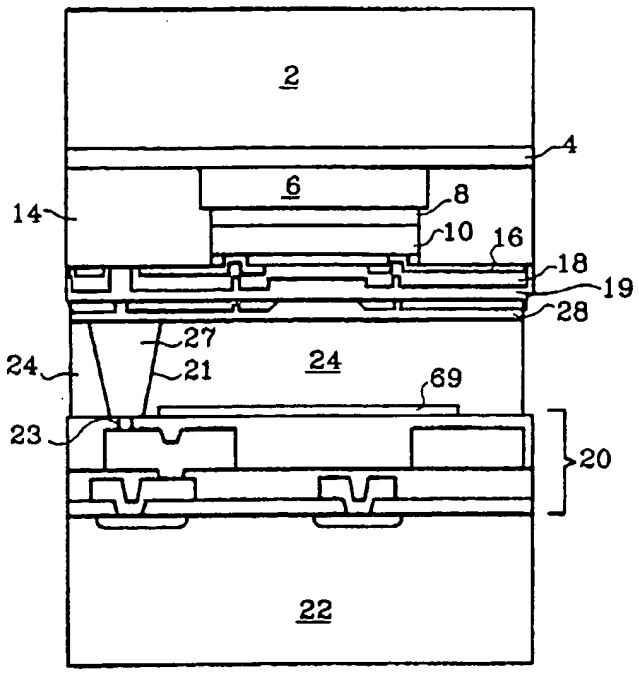

Fig.11

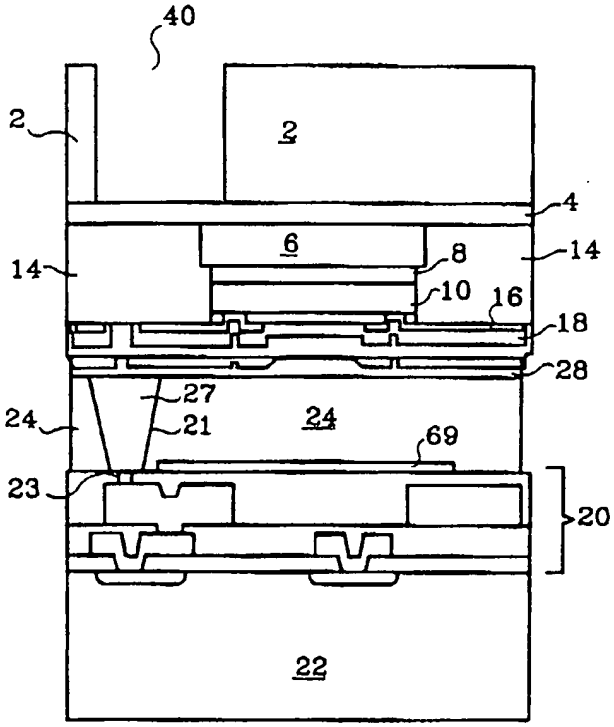

Fig.12

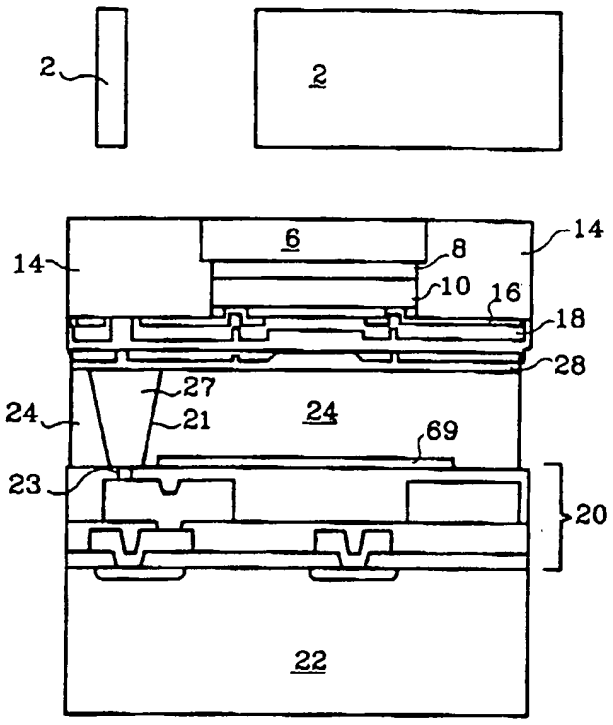

Fig.13

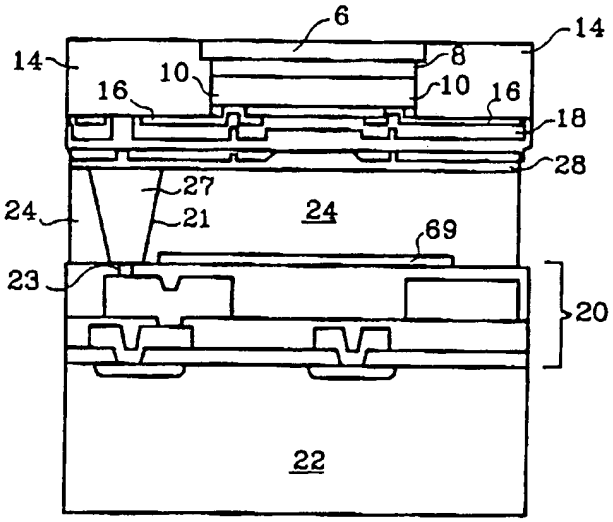

Fig.14

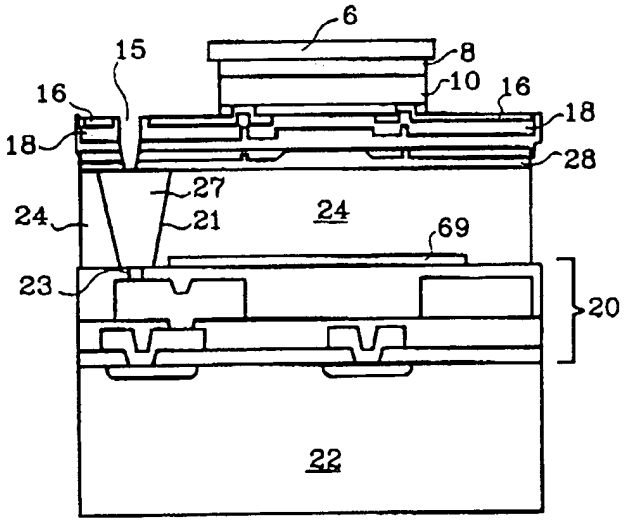

Fig.15

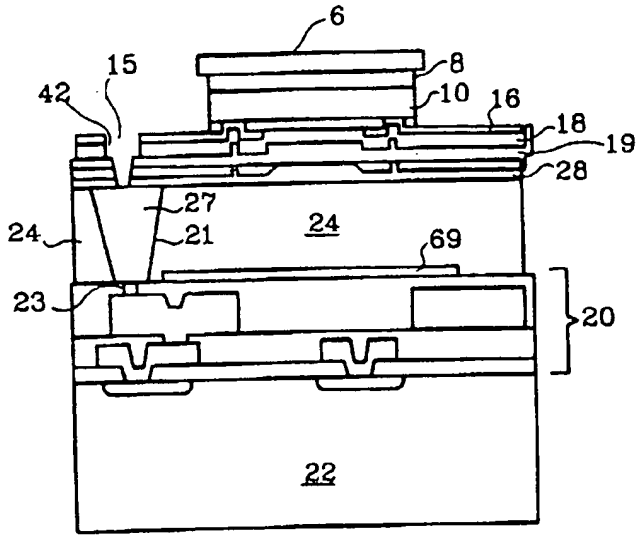

Fig.16

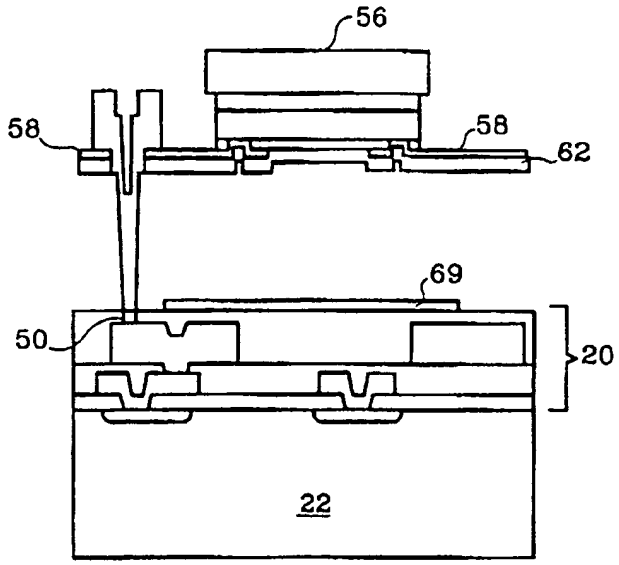

Fig.27

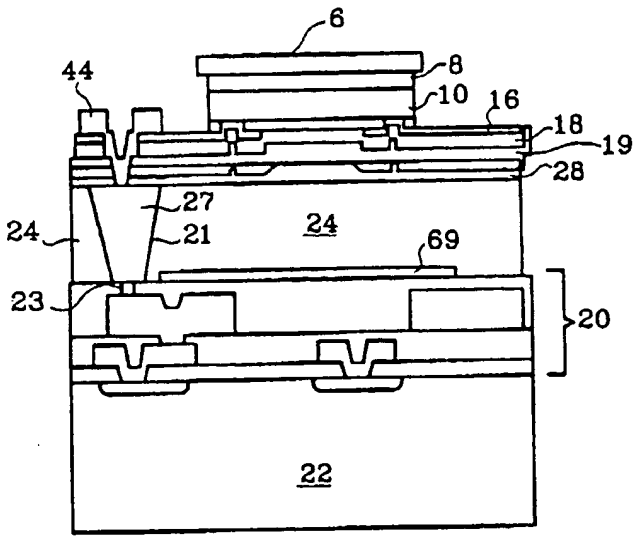

Fig.17

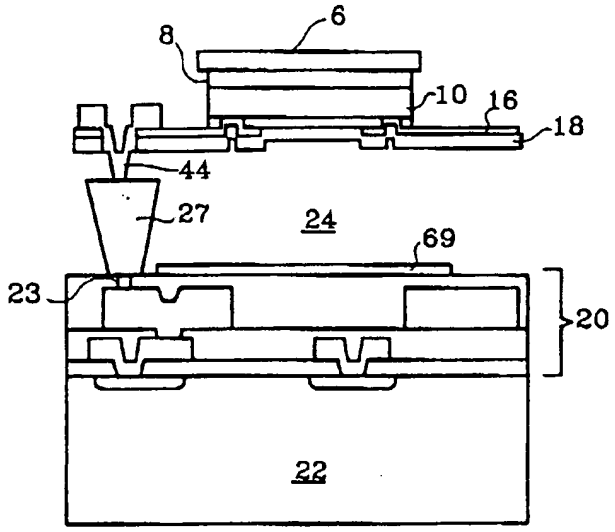

Fig.18

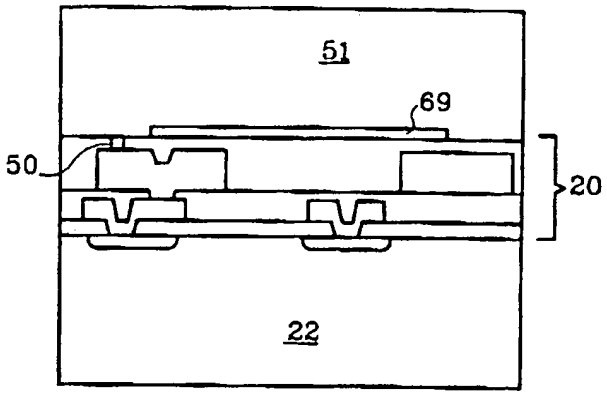

Fig.19

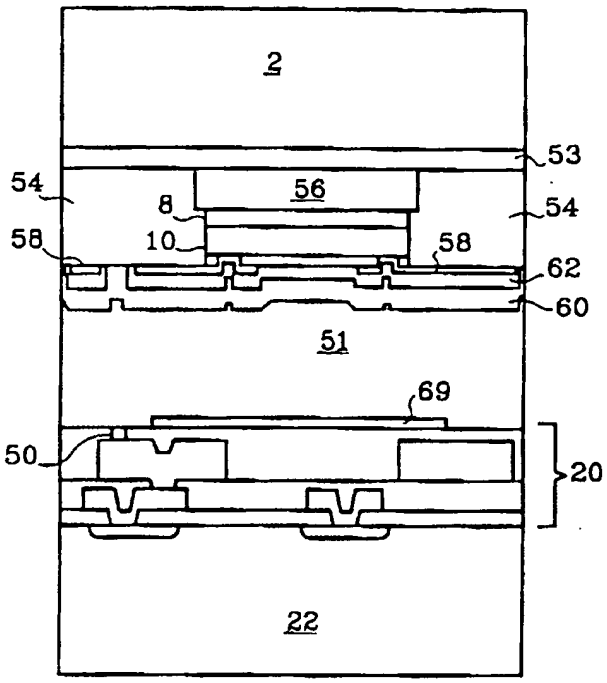

Fig.20

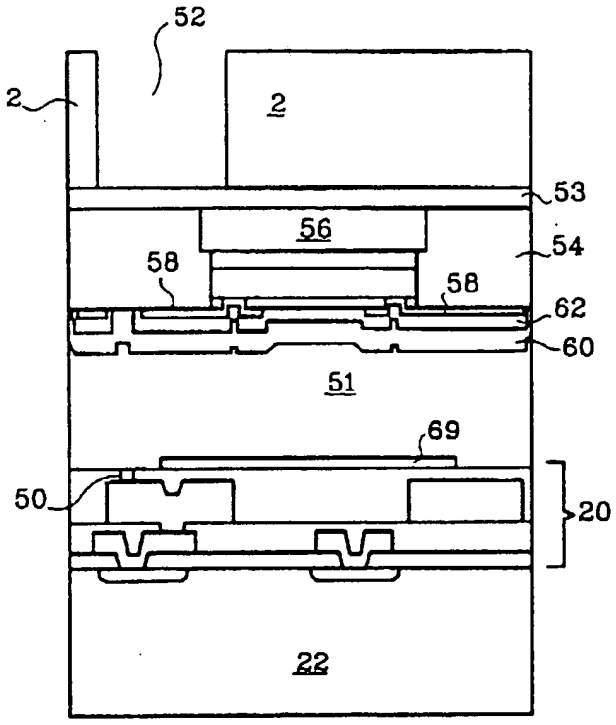

Fig.21

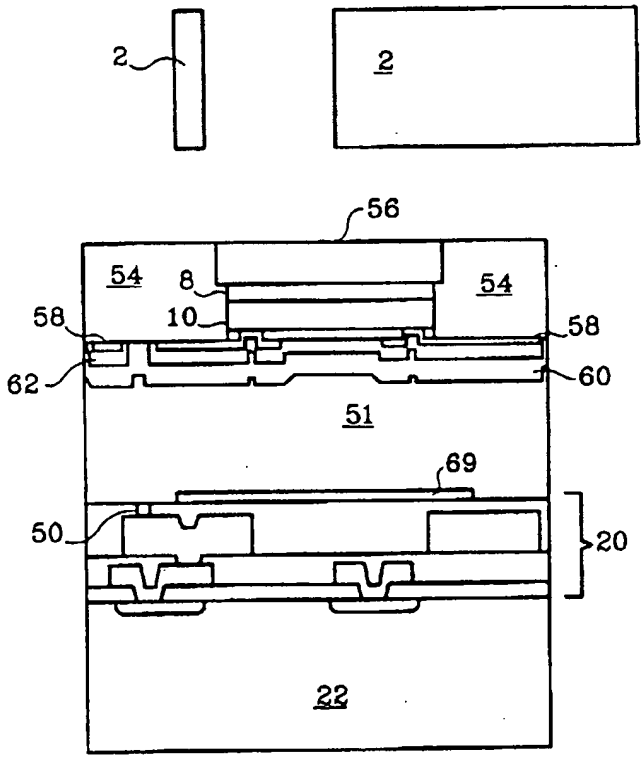

Fig.22

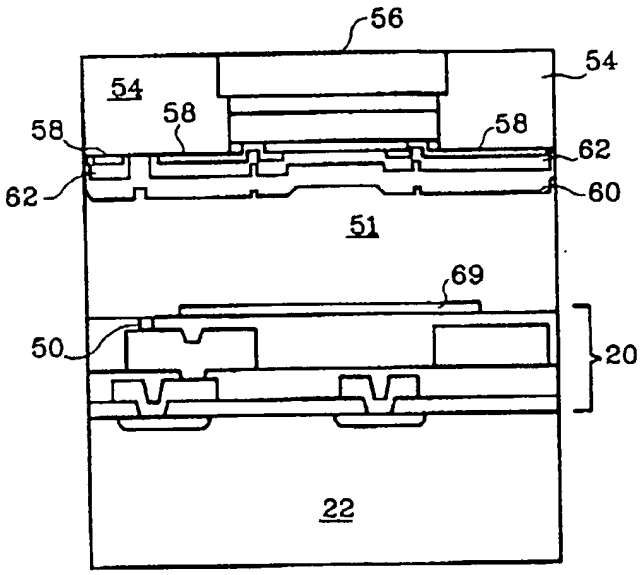

Fig.23

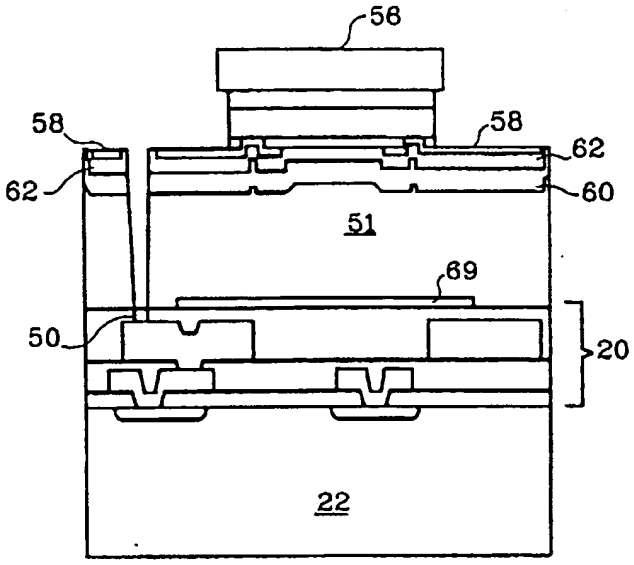

Fig.24

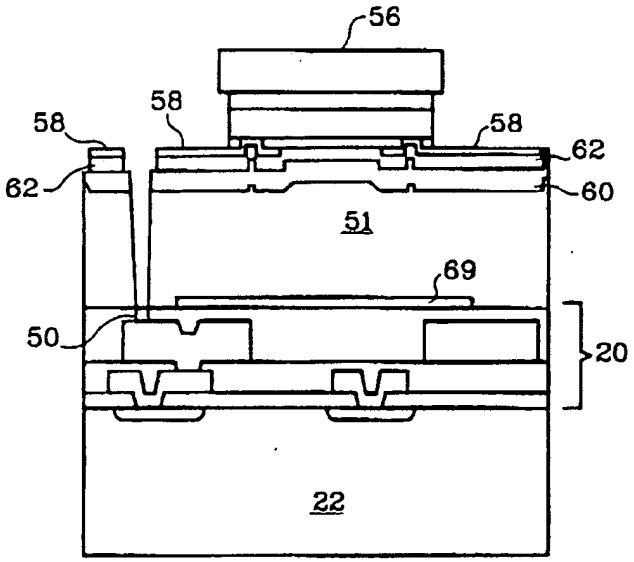

Fig.25

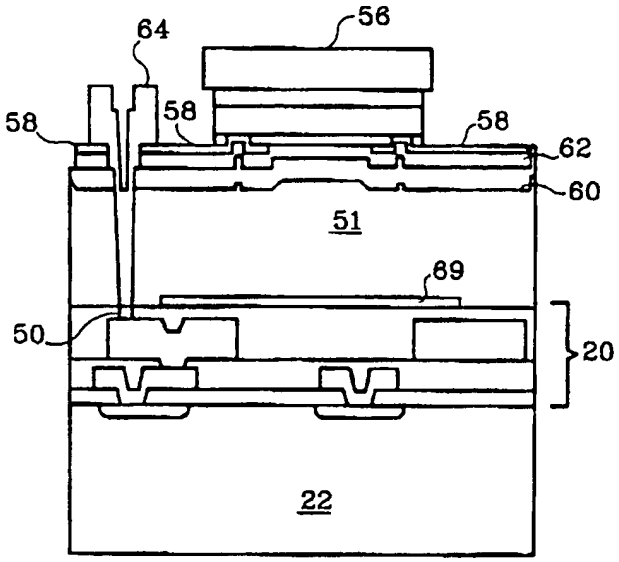

Fig.26

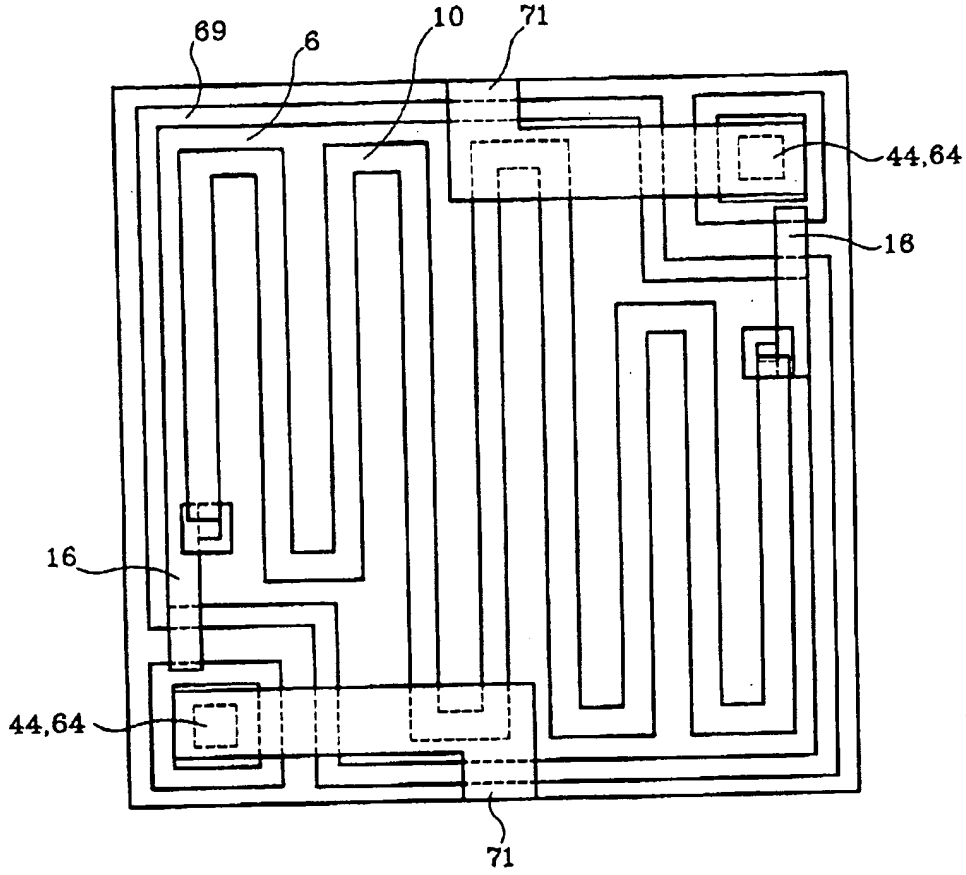

Fig.28

INTERNATIONAL SEARCH REPORT

Interr. nal Application No
PCT/US 00/21031

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/98 H01L25/065 G01J5/20 G01K7/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G01J G01K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 627 106 A (HSU CHEN-CHUNG) 6 May 1997 (1997-05-06) column 2, line 44 -column 4, line 19; figures 2-12	1,4-9
Y		2,3, 10-16

Y	COLE B ET AL: "MONOLITHIC TWO-DIMENSIONAL ARRAYS OF MICROMACHINED MICROSTRUCTURES FOR INFRARED APPLICATIONS" PROCEEDINGS OF THE IEEE,US,IEEE. NEW YORK, vol. 86, no. 8, August 1998 (1998-08), pages 1679-1686, XP000848433 ISSN: 0018-9219 the whole document	2,3, 10-16

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search	Date of mailing of the international search report
12 December 2000	20/12/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Munnix, S

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INTERNATIONAL SEARCH REPORT

Intern. nal Application No
PCT/US 00/21031

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 02, 26 February 1999 (1999-02-26) -& JP 10 303434 A (MURATA MFG CO LTD), 13 November 1998 (1998-11-13) abstract	1-16
A	US 5 572 060 A (CELIK-BUTLER ZEYNEP ET AL) 5 November 1996 (1996-11-05) column 3, line 45 - line 55 column 6, line 38 -column 7, line 37 figure 1	1-16
A	US 5 173 474 A (CONNELL GEORGE A N ET AL) 22 December 1992 (1992-12-22) abstract	2,3
A	US 5 465 009 A (DRABIK TIMOTHY J ET AL) 7 November 1995 (1995-11-07) column 3, line 29 -column 5, line 8 column 6, line 13 - line 35 column 6, line 51 - line 60 column 8, line 26 - line 55	12,13
A	US 5 246 880 A (REELE SAMUEL ET AL) 21 September 1993 (1993-09-21) the whole document	14,15

3

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr. ›nal Application No
PCT/US 00/21031

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5627106 A	06-05-1997	NONE	
JP 10303434 A	13-11-1998	NONE	
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		CA 2212002 A	08-08-1996
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		US 5850098 A	15-12-1998
		WO 9624165 A	08-08-1996
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US 5465009 A	07-11-1995	US 5286335 A	15-02-1994
US 5246880 A	21-09-1993	NONE	

cut in metal 16 should be enough to allow deposition of a contact structure later in the process. A dielectric 18 providing passivation of the metal 16 is deposited.

Dielectric 18 is patterned and removed in the region of space 15, providing direct access to polyimide layer 14 from the surface of the microstructure. Figure 5 shows this structure.

Finally, a polyimide layer 19 is deposited across the surface to a depth of about 1000 angstroms, extending to the previously deposited polyimide layer 14 and to a height greater than the depth of space 15. This wafer and its microstructures now undergo thermal processing to about 100 degrees C in order to partially cure polyimide layer 14. See Figure 6. At this point, the fabrication of the sensor itself is complete.

In the second phase, the readout or drive electronics are formed on a wafer 22 using standard CMOS processes. An electronic connection is formed at the top level of the CMOS devices in order to make electrical contact with a microstructure that is formed in phase one. The present wafer carries a thick layer of sacrificial bonding material which when removed, with the thin polyimide layer on the other wafer, provides a cavity for thermal isolation of the CMOS devices from the microstructure and for optical reflection. These process steps are shown in Figures 7-10.